

C. REMARKS**Status of the Claims**

Claims 1, 3-8, 18, 20, and 22-30 are currently present in the Application, and claims 1, 18, and 25 are independent claims. Claims 1, 8, 18, and 25 have been amended, claims 11, 13, and 15-17 have been cancelled, and no claims have been added in this response. Applicants are not conceding in this Application that the canceled claims are not patentable over the art cited by the Examiner, as the present claim cancellations are only for facilitating expeditious prosecution of the Application. Applicants respectfully reserve the right to pursue these and other claims in one or more continuation and/or divisional patent applications.

Examiner Interview

Applicants note with appreciation the telephonic interview conducted between Applicants' representative and the Examiner on June 12, 2006. During the telephonic interview and follow-up phone calls, the Examiner and Applicants' representative discussed amendments to overcome the art of record. The Examiner suggested that by including limitations focused on private and non-private memory areas, such amendment would read over the art of record. These amendments are included in this response.

Claim Rejections

Claims 1, 3-8, 11, 13, 15-18, 20, and 22-30 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Auslander et al. (U.S. Pat. No. 6,601,146, hereinafter "Auslander") in view of Schwarm et al. (U.S. Pat. No. 6,813,522, hereinafter "Schwarm"). Applicants respectfully traverse these rejections.

Claims 11, 13, and 15-17 have been canceled in this response and, therefore, rejections to these claims are moot.

Applicants have amended Applicants' independent claims to include limitations that further describe private and non-private memory areas. Support for such amendment may be found in Applicants' specification on page 48 line 24 through page 49 line 15. Therefore, no new matter is added with such amendment. As amended, claim 1 is directed to a memory shared by a plurality of heterogeneous processors with limitations comprising:

- the shared memory;
- wherein the shared memory is accessible by one or more first processors that are adapted to process a first instruction set;
- wherein the shared memory is accessible by one or more second processors that are adapted to process a second instruction set;
- wherein the shared memory is partitioned into a non-private memory area that is accessible by one or more of the first processors and one or more of the second processors;
- wherein one of the second processors is adapted to access a private memory area that is not accessible by any of the first processors; and
- a memory map corresponding to the shared memory, wherein the memory map includes cross-references between virtual addresses and real addresses, the memory map and the cross-references shared between the first processors and the second processors.

Amended claim 1 includes limitations of "*wherein the shared memory is partitioned into a non-private memory area that is accessible by one or more of the first processors and one or more of the second processors*" and "*wherein one of the second processors is adapted to access a private memory area that is not accessible by any of the first processors.*" In contrast,

while Auslander and Schwarm disclose different processor types being able to access a shared memory area, neither Auslander nor Schwarm disclose that one processor type is also able to access a private memory area while another processor type is not able to access the private memory area. Specifically, Auslander and Schwarm state:

"With this invention, a memory region called the IPC transfer region is shared among all processes of the system to enable more efficient IPC." (Auslander, Abstract)

"Then, in step 62 the boot processor copies data from the boot data region (43 in FIG. 3) to the clone data regions (e.g., 45 in FIG. 3)." (Schwarm, col. 8, lines 31-33)

As can be seen from the above excerpts, and agreed upon by the Examiner, neither Auslander nor Schwarm, either alone or in combination with each other, teach or suggest *"wherein the shared memory is partitioned into a non-private memory area that is accessible by one or more of the first processors and one or more of the second processors"* and *"wherein one of the second processors is adapted to access a private memory area **that is not accessible** by any of the first processors"* as claimed by Applicants.

In addition, Applicants claim *"wherein the memory map includes cross-references between virtual addresses and real addresses, the memory map and the cross-references shared between the first processors and the second processors."* Regarding Auslander, Auslander uses different cross-references for the different processors. Specifically, Auslander states:

"To achieve this, a different physical address for the IPC Transfer Region is chosen for each processor. Thus, when a process is migrated from one processor to another, the operating system must change the mapping of the IPC Transfer Region virtual address so that it

points to the appropriate physical address for that processor." (page 4, lines 15-23)

Likewise, Swarm also uses different memory maps for each processor. Swarm states:

"...each of the processors has **a respective address translator** 32, 33, 34, that permits the respective processors to execute the same read-write access instructions in the shared program for accessing respective different regions of the shared memory." (col. 5, lines 23-25)

As can be seen from the above excerpts, neither Auslander nor Swarm, either alone or in combination with each other, teach or suggest *"wherein the memory map includes cross-references between virtual addresses and real addresses, the memory map and the cross-references shared between the first processors and the second processors"* as claimed by Applicants.

Therefore, since neither Auslander nor Swarm teach or suggest, either alone or in combination with each other, all the limitations included in Applicants' claim 1 as amended, amended claim 1 is allowable over Auslander in view of Swarm. Claim 18 is a computer program product claim including similar limitations of claim 1 and, therefore, is allowable for at least the same reasons that claim 11 is allowable. Claim 25 is a system claim including similar limitations of claim 1 and, therefore, is allowable for at least the same reasons that claim 11 is allowable.

Notwithstanding the fact that claim 30 is dependent upon claim 1 and, therefore, allowable for at least the same reasons as claim 1, claim 30 adds the limitation to claim 1 of:

- wherein the shared memory, the first processors, and the second processors are included on one silicon substrate and are connected using an on chip coherent multi-processor bus.

The Office Action never points to a particular excerpt in Auslander or Schwarm to reject Applicants' claim 30 limitation. After further review however, neither Auslander nor Schwarm teach or suggest, either alone or in combination with each other, *"wherein the shared memory, the first processors, and the second processors are included on one silicon substrate and are connected using an on chip coherent multi-processor bus"* as claimed by Applicants. Therefore, claim 30 is allowable over Auslander in view of Schwarm.

Each of the remaining claims 3-8, 20, 22-24, and 26-29 each depend upon one of the allowable independent claims 1, 11, 18, or 25. Therefore, each of claims 3-8, 13, 15-17, 20, 22-24, and 26-29 are allowable for at least the same reasons that their respective independent claim is allowable.

Conclusion

As a result of the foregoing, it is asserted by Applicants that the remaining claims in the Application are in condition for allowance, and Applicants respectfully request an early allowance of such claims.

Applicants respectfully request that the Examiner contact the Applicants' attorney listed below if the Examiner believes that such a discussion would be helpful in resolving any remaining questions or issues related to this Application.

Respectfully submitted,

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